REMARKS

The claims have not been amended. Accordingly, claims 1-16 are currently pending in the application, of which claims 1 and 9 are independent claims.

Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Rejections Under 35 U.S.C. § 103

Claims 1 and 3-8 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,366,025 issued to Yamada ("Yamada"). Applicants respectfully traverse this rejection for at least the following reasons.

To establish an obviousness rejection under 35 U.S.C. § 103(a), four factual inquiries must be examined. The four factual inquiries include (a) determining the scope and contents of the prior art; (b) ascertaining the differences between the prior art and the claims in issue; (c) resolving the level of ordinary skill in the pertinent art; and (d) evaluating evidence of secondary consideration. *Graham v. John Deere*, 383 U.S. I, 17-18 (1966). In view of these four factors, the analysis supporting a rejection under 35 U.S.C. 103(a) should be made explicit, and should "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed. *KSR Int'l. Co. v. Telefex, Inc.*, 550 U.S. __, slip op. at 14-15 (2007). Furthermore, even if the prior art may be combined in the manner claimed, there must be a reasonable expectation of success, and the reference or references, when combined, must disclose or suggest all of the claim limitations. *See in re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The Examiner has failed to establish a *prima facie* case of obviousness because Yamada fails to teach or suggest every feature of claim 1. Specifically, claim 1 recites, *inter alia*:

wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region with a different geometric structure between the multi gates from one another.

Yamada fails to teach or suggest at least these features of claim 1. The Examiner states, "The transistors are not taught directly but it is inherent for a pixel to have a transistor. It would be obvious for each pixel R, G, and B to contain subpixels of R, G, and B to form unit pixels as described in claim 1" (Office Action, page 3). However, each of the claimed transistors includes an offset region with a different geometric structure between the multi gates from one another. There is nothing in Yamada that teaches or suggests transistors having the claimed offset regions, and the Examiner has failed to provide any reason why the claimed transistor configuration is obvious.

It is further noted that, as explained in the previous response, emissive areas 1B, 1R, and 1G fail to teach any characteristics of the transistors in the pixels. Rather, Yamada states that Figure 5 shows "[t]he basic cross-sectional configuration of each R, G, and B display pixel." (col. 6, lines 53-54; emphasis added). Consequently, although Yamada teaches different sized emissive areas in the pixels, the first TFT 30 and the second TFT 40 respectively have the same configuration in the red, green, and blue pixels. Accordingly, Yamada fails to teach or suggest at least "wherein transistors of at least two unit pixels of the R, G, and B unit pixels each include a offset region with a different geometric structure between the multi gates from one another."

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claim 1. Claims 3-8 depend from claim 1 and are allowable at least for this reason. Since none of the other prior art of record discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 1, and all the claims that depend therefrom, are allowable.

Claims 2 and 9-12 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Yamada in view of U.S. Patent No. 6,529,213 issued to Kimura ("Kimura"). Applicants respectfully traverse this rejection for at least the following reasons.

Applicants respectfully submit that claim 2 is allowable over Yamada and Kimura fails to cure the deficiencies of Yamada noted above with regard to claim 1. Hence, claim 2 is allowable at least because it depends from an allowable claim 1.

With regard to claims 9-12, the Examiner has failed to establish a *prima facie* case of obviousness. Claim 9 recites, *inter alia*:

> wherein transistors of at least two unit pixels among the R, G, and B unit pixels each include an offset region having a different resistance value between the multi gates from one another

Yamada in view of Kimura fails to teach or suggest at least this feature of claim 9. As discussed above, Yamada discloses pixels having different light emitting areas, but not transistors having different offset regions. Kimura fails to cure this deficiency in Yamada.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claim 9. Claims 10-12 depend from claim 9 and are allowable at least for this reason. Since none of the other prior art of record, whether taken alone or in any combination, discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 9, and all the claims that depend therefrom, are allowable.

Claims 13-16 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Yamada in view of Kimura, further in view of U.S. Patent No. 6,278,130 issued to Joo, *et al.* ("Joo"). Applicants respectfully traverse this rejection for at least the following reasons.

Applicants respectfully submit that claim 9 is allowable over Yamada and Kimura and Joo fails to cure the deficiencies of Yamada and Kimura noted above with regard to claim 9. Hence, claims 13-16 are allowable at least because they depend from an allowable claim 9.

CONCLUSION

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submit that all of the grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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